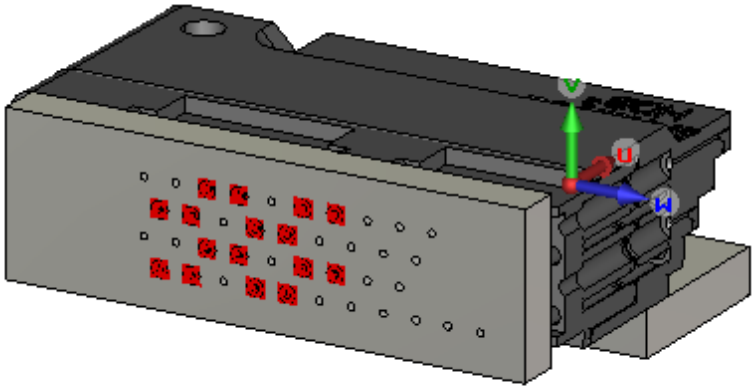
Amphenol

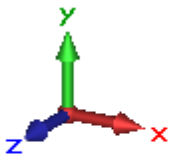
HSB3 Signal Integrity Analysis

All Rows, De-populated (No Grounds)

Interconnect Technology

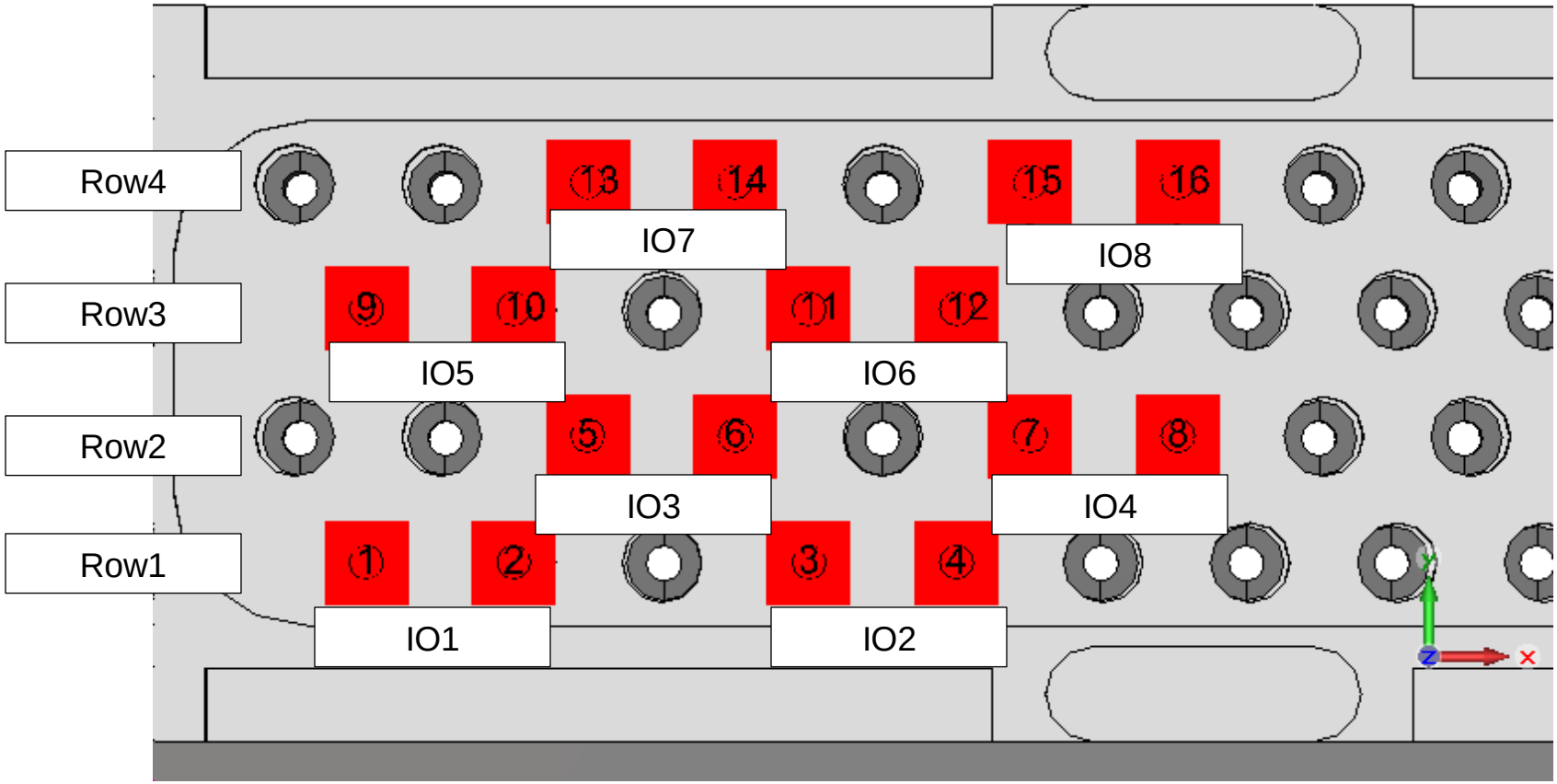
HSB3 (No Grounds) CST 3D Model





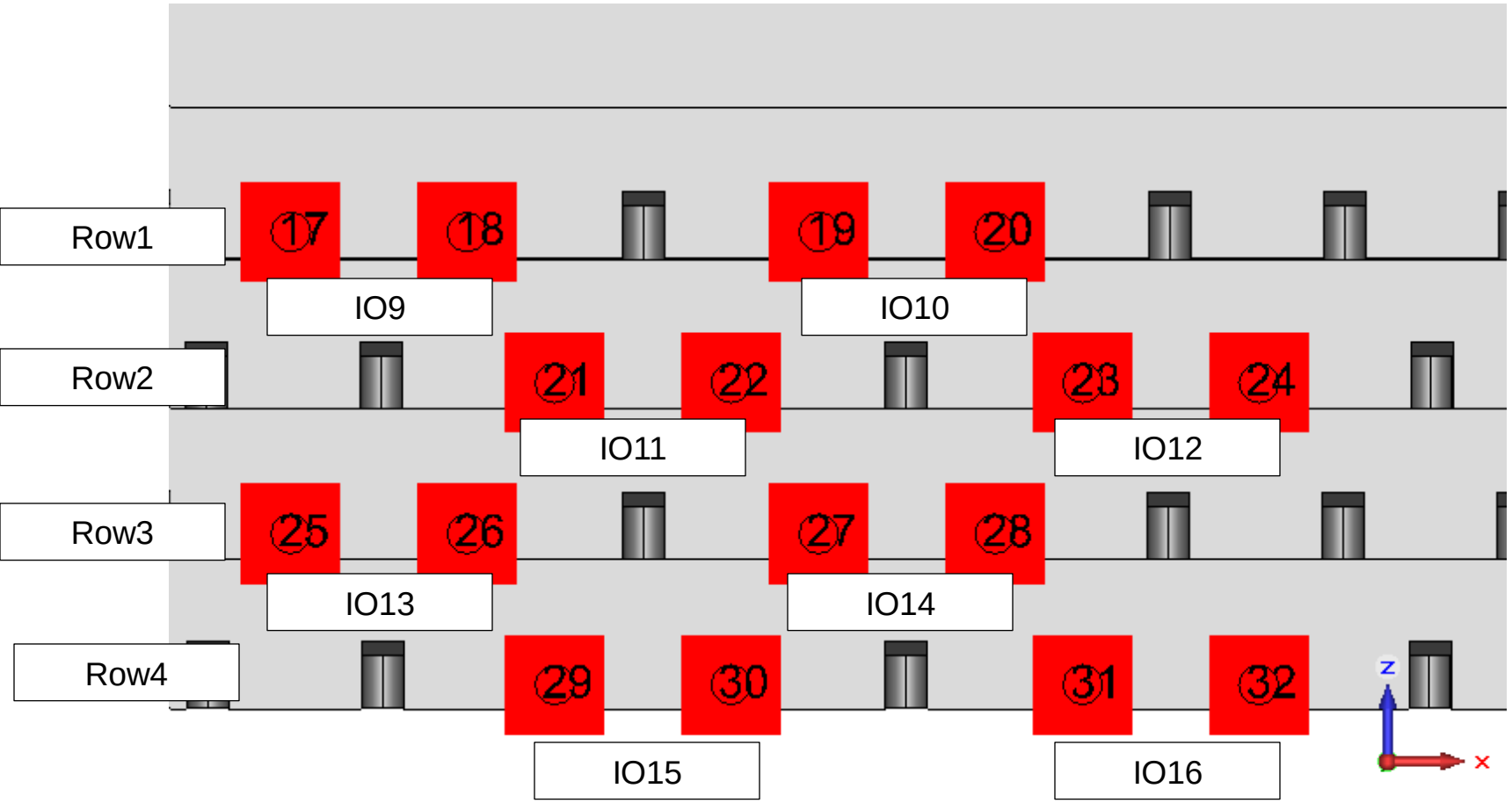
Backplane Port Numbering

(IO1 thru 7 are corresponding mixed mode ports on Test Bed and Channel simulation schematics)



Daughter Card Port Numbering

(IO9 thru 16 are corresponding mixed mode ports on Test Bed and Channel simulation schematics)

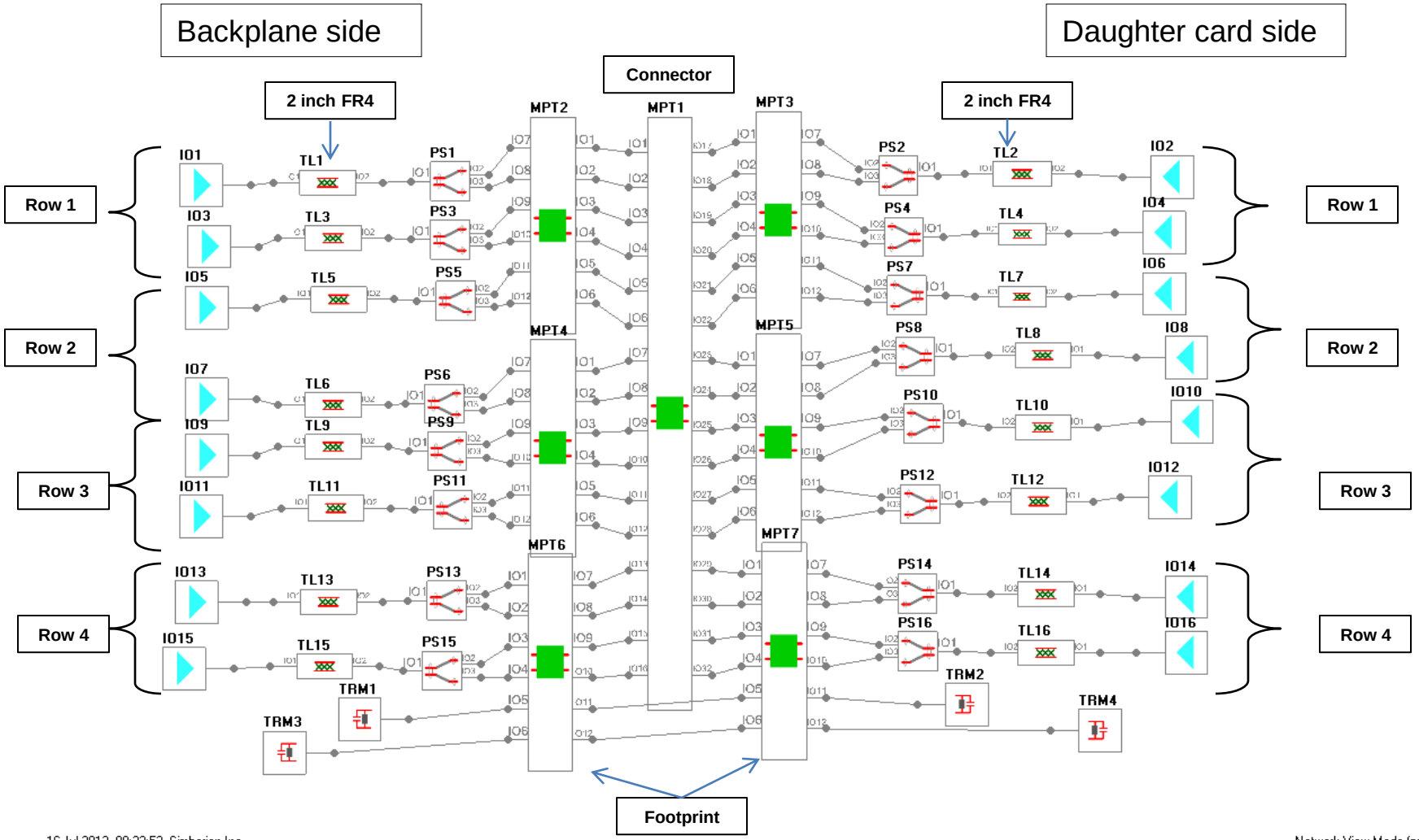


Test Bed Simulation Schematic

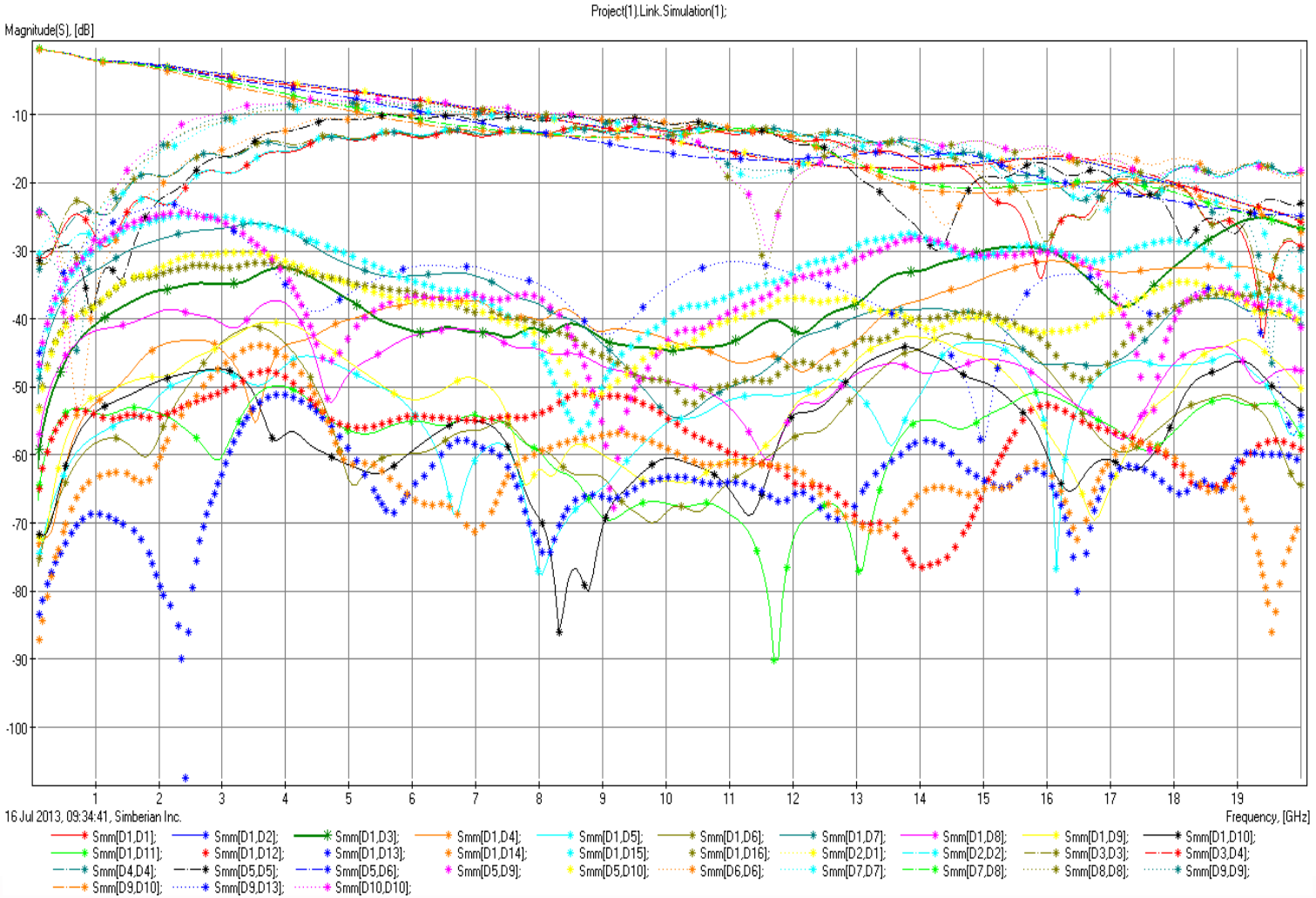
PS 1 thru 32 are single ended to differential convertors.

IO1 thru 16 are Mixed Mode ports.

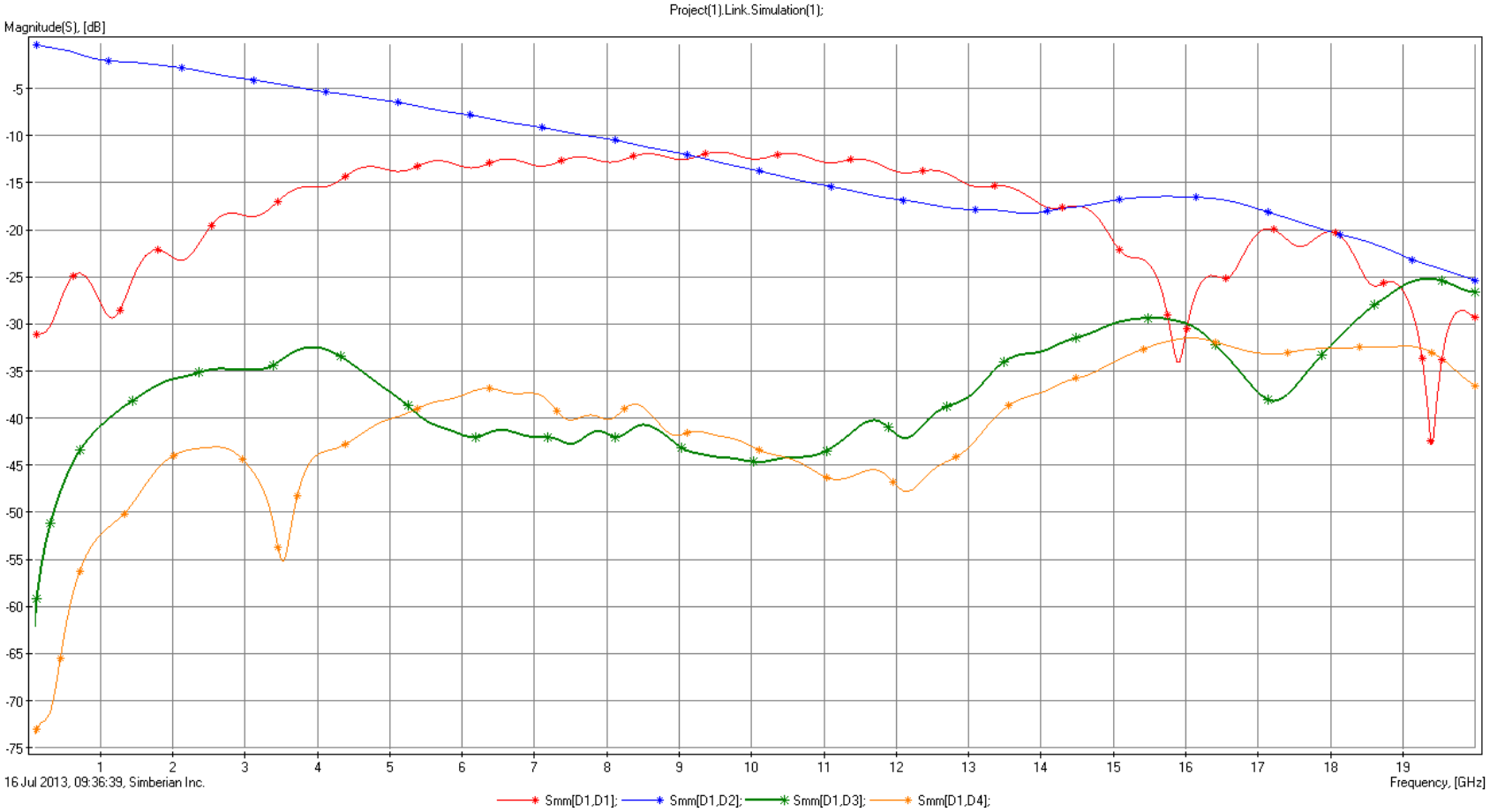
TRM1 thru 4 are ideal 50 ohm terminations for unused footprint ports.



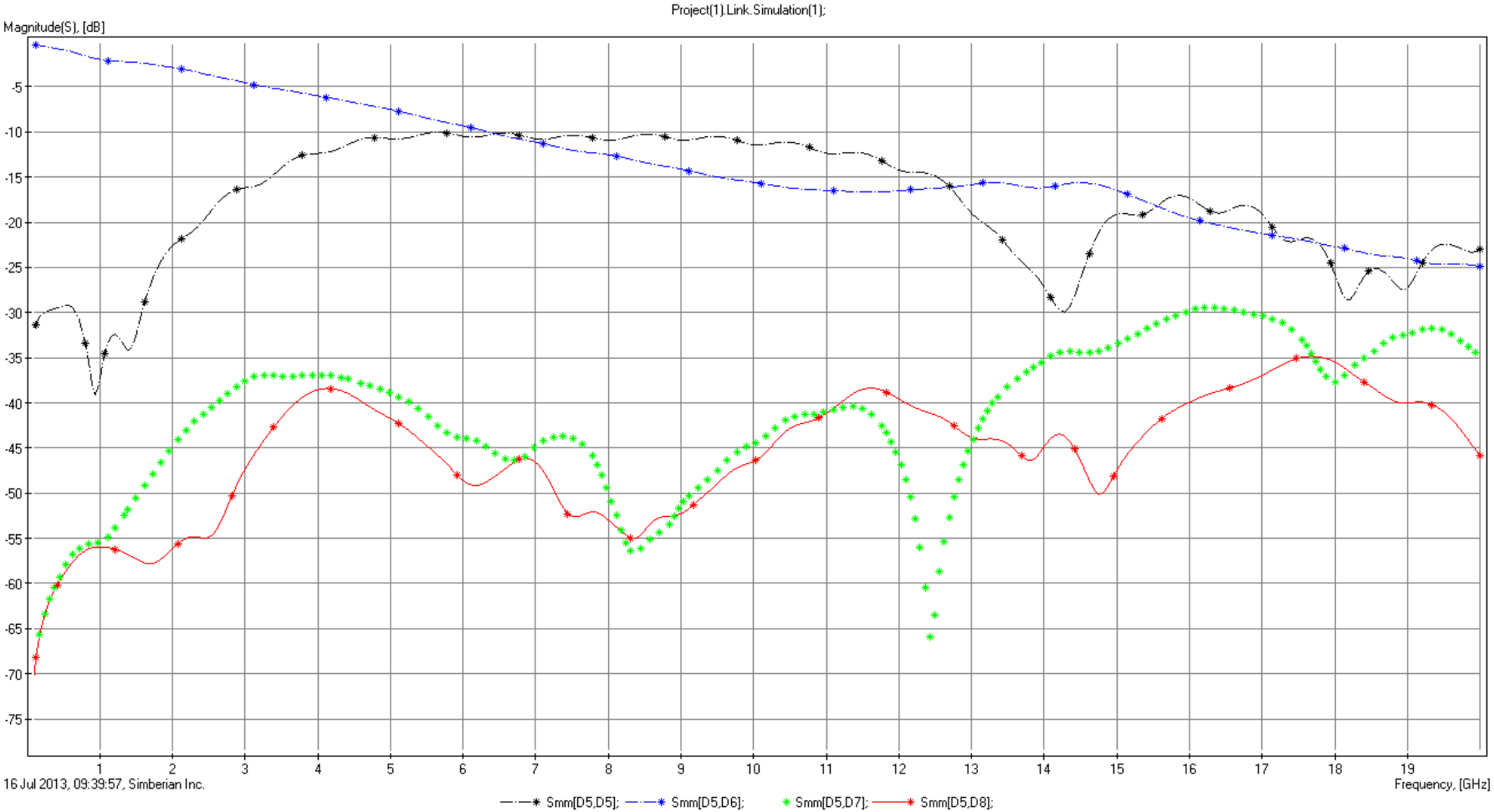
General S Parameters



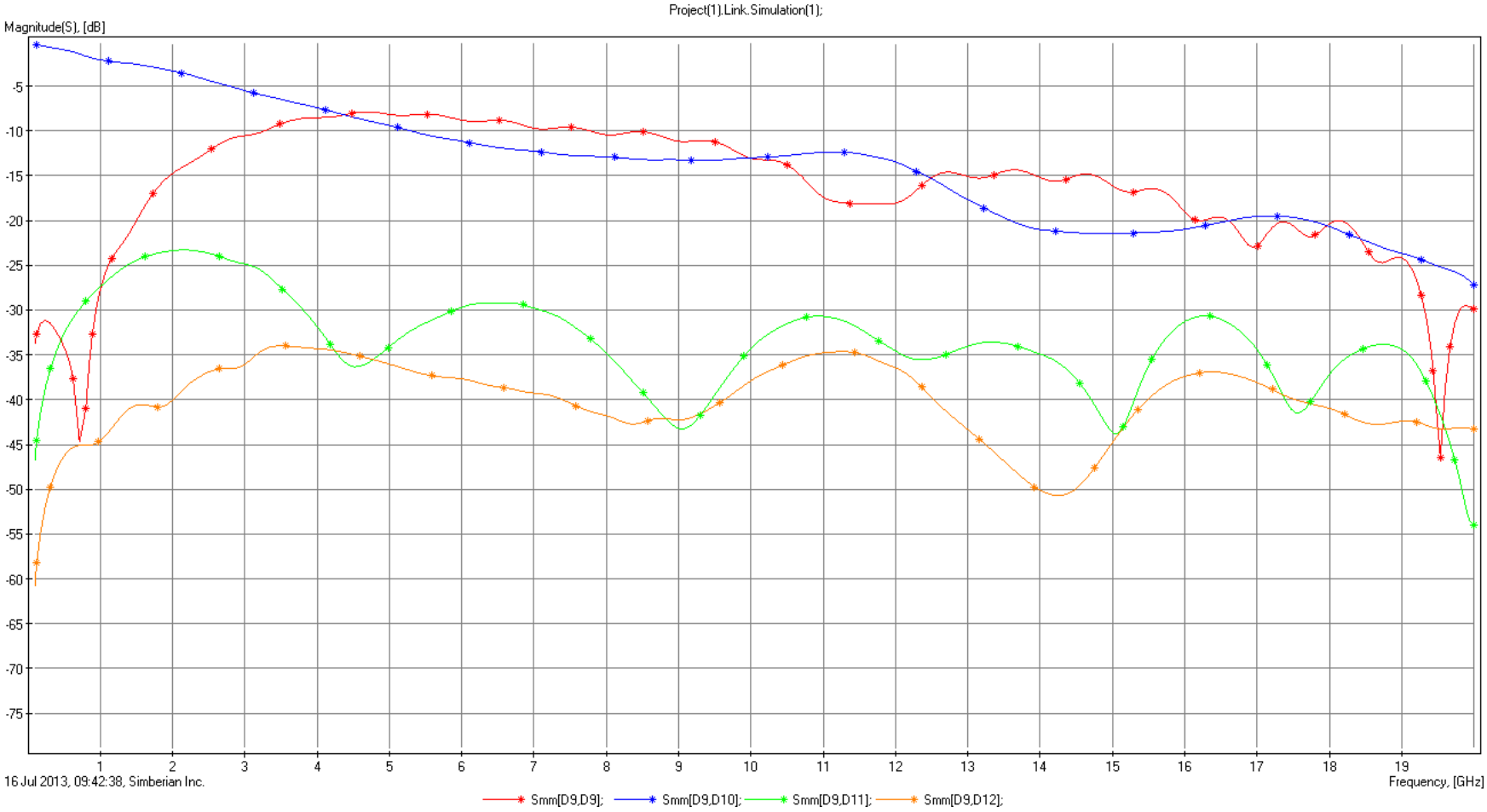
S Parameters – Row 1



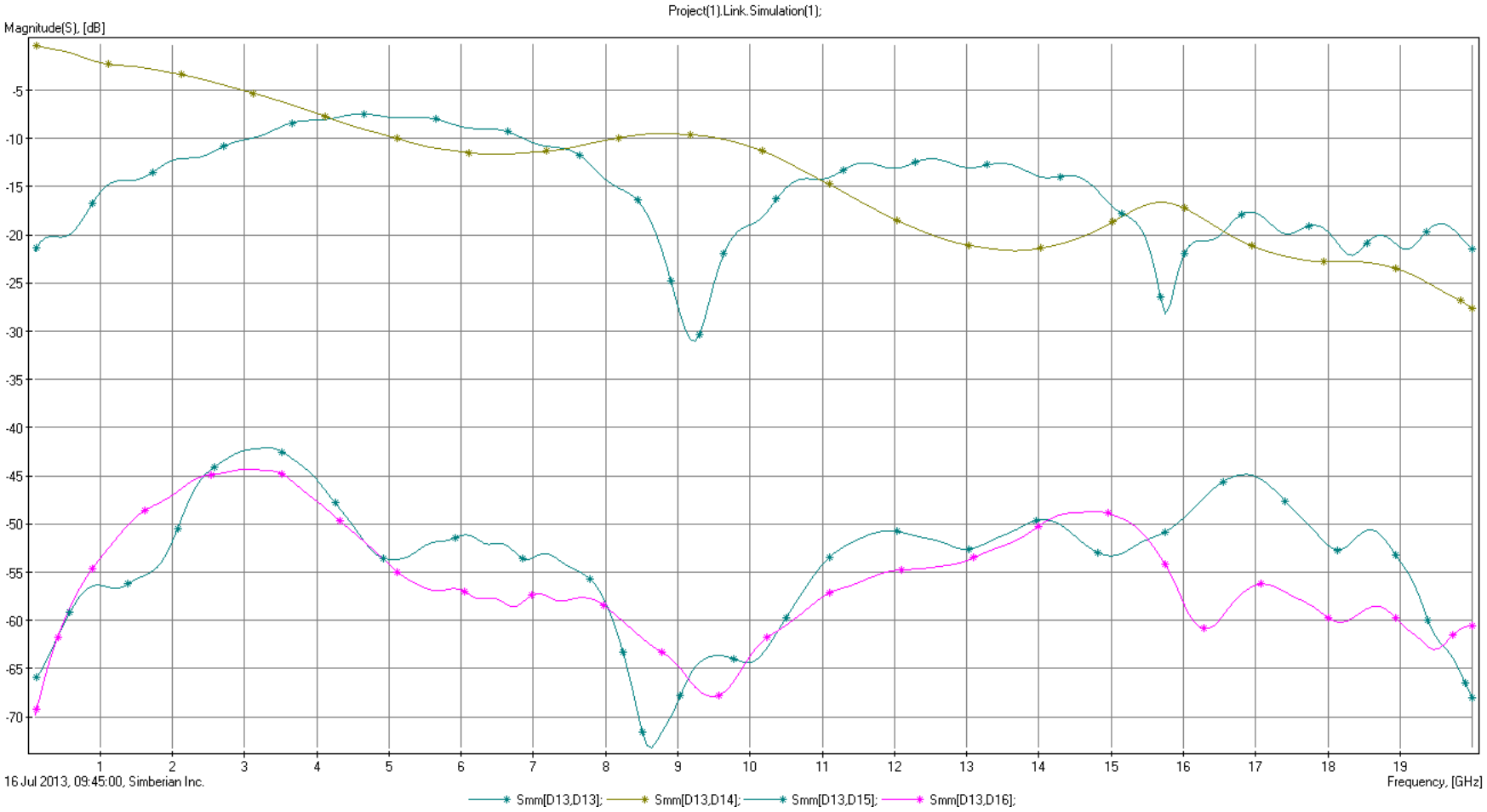
S Parameters – Row 2



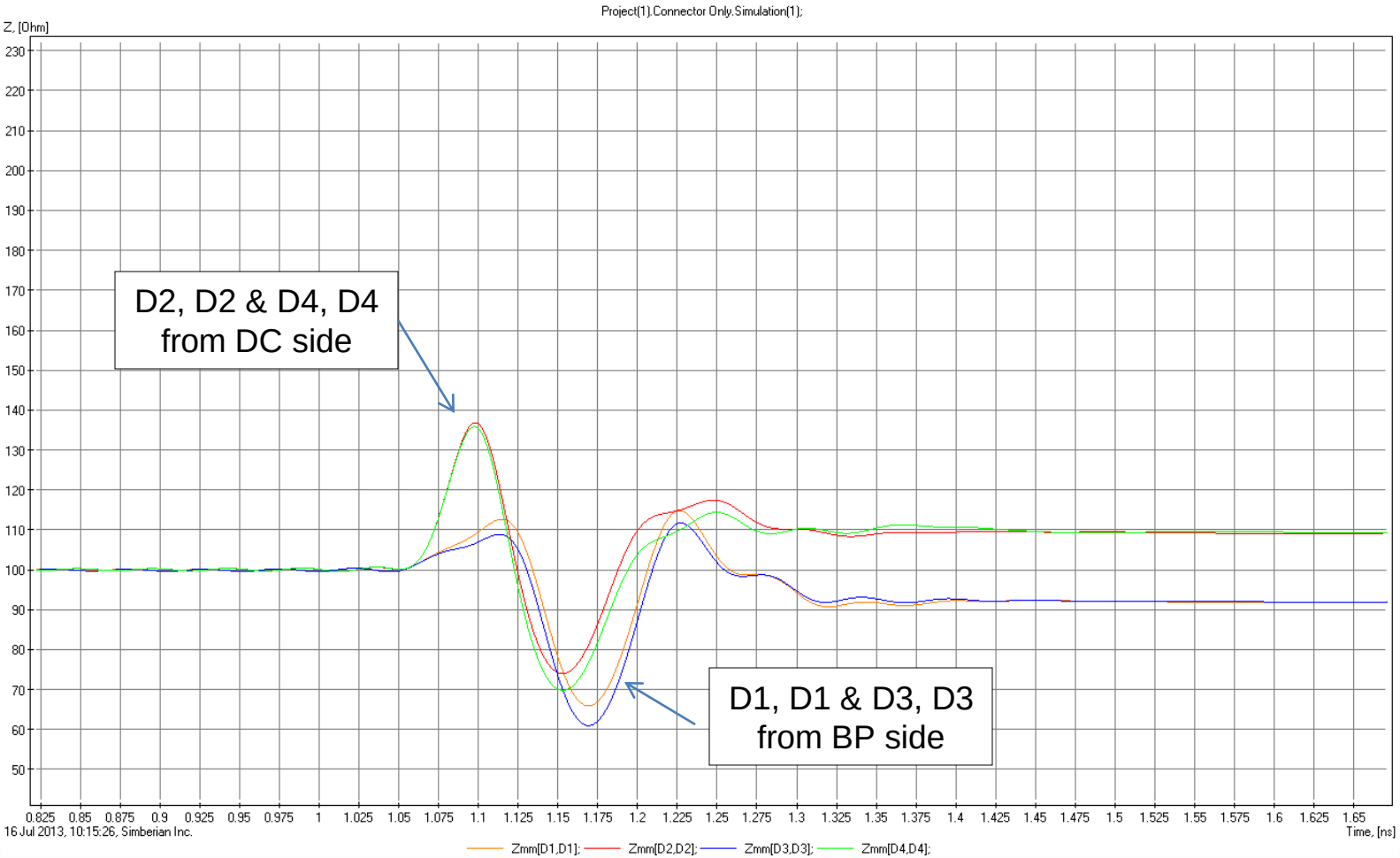
S Parameters – Row 3



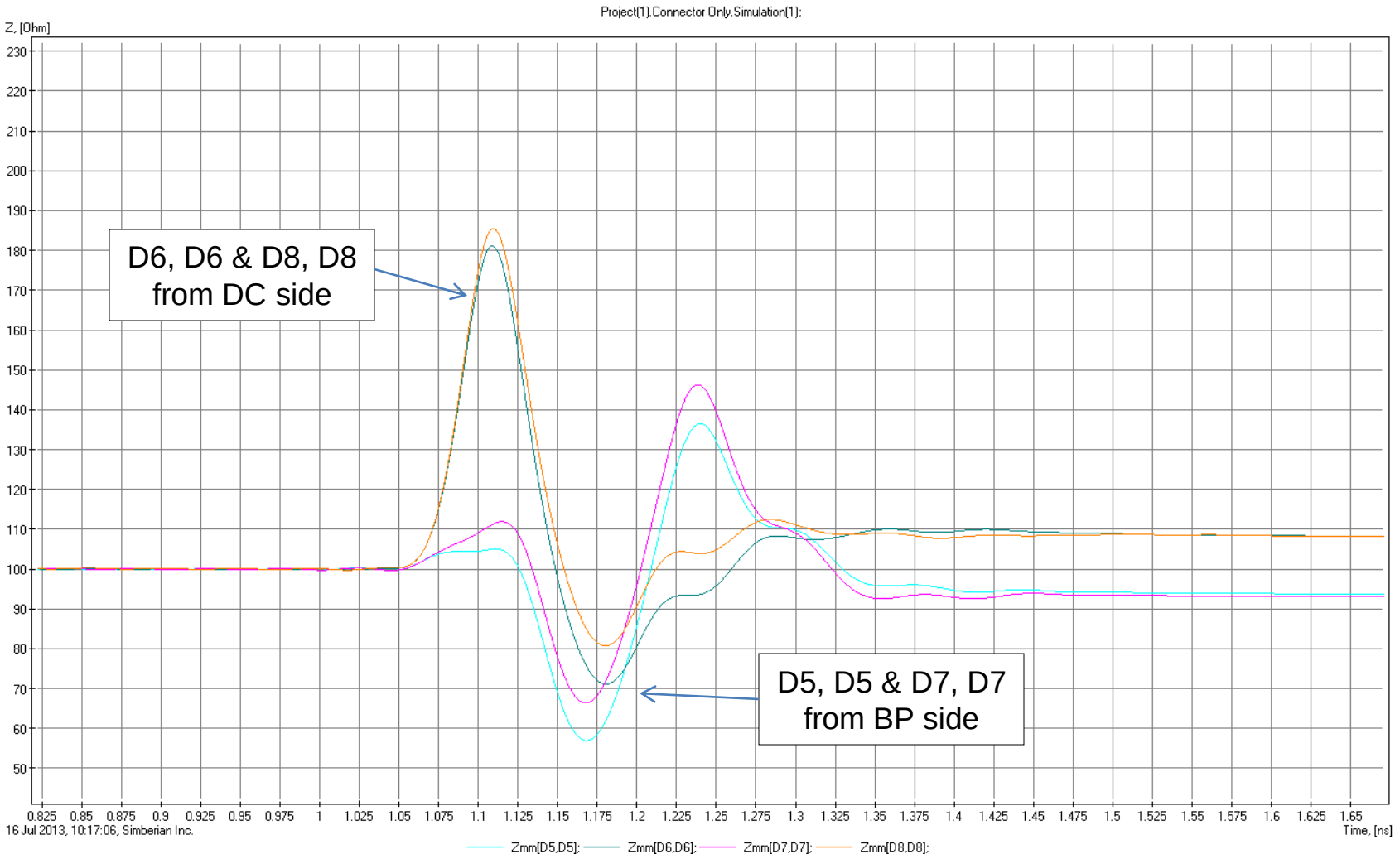
S Parameters – Row 4



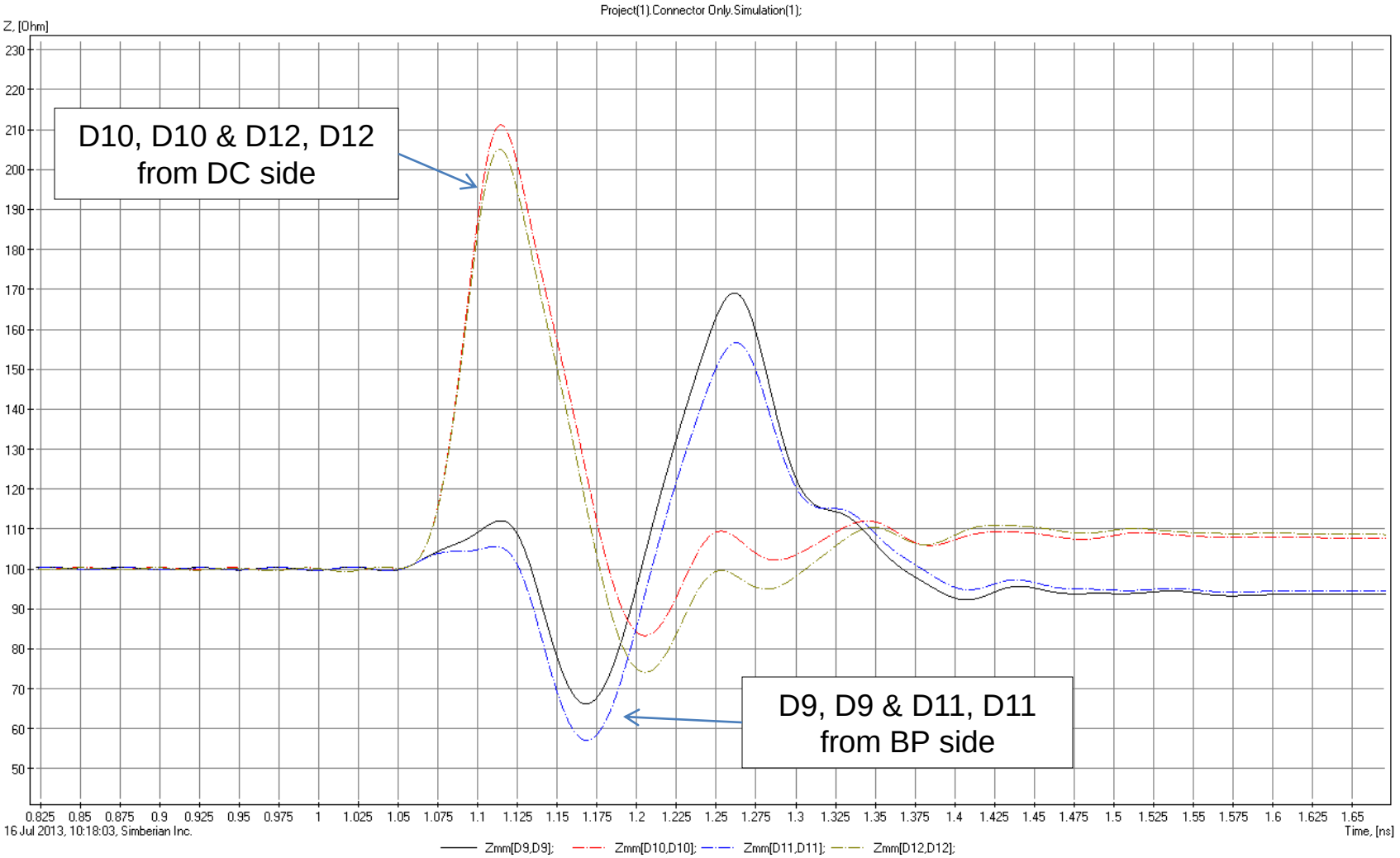
Connector TDR Profile – Row 1



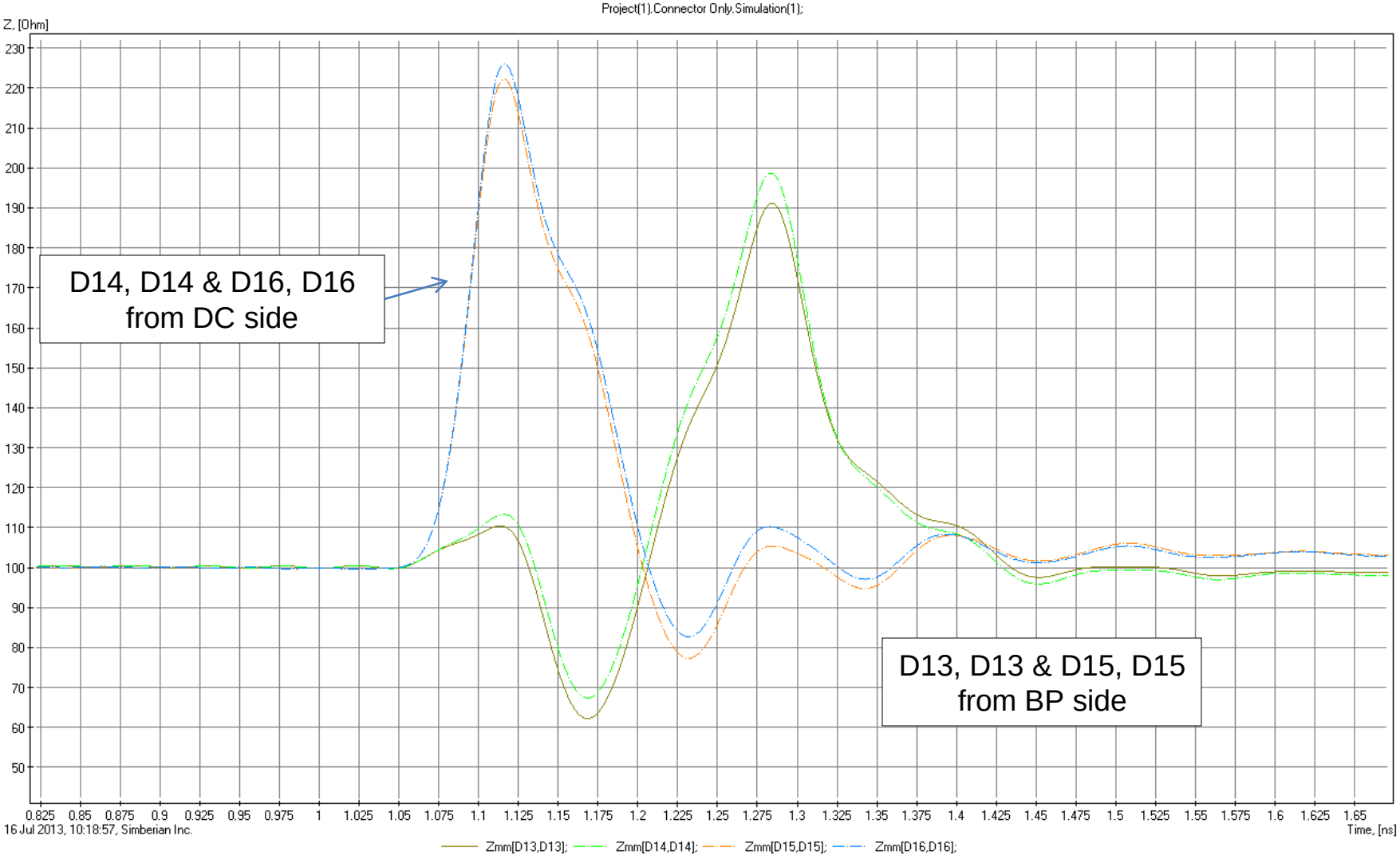
Connector TDR Profile – Row 2



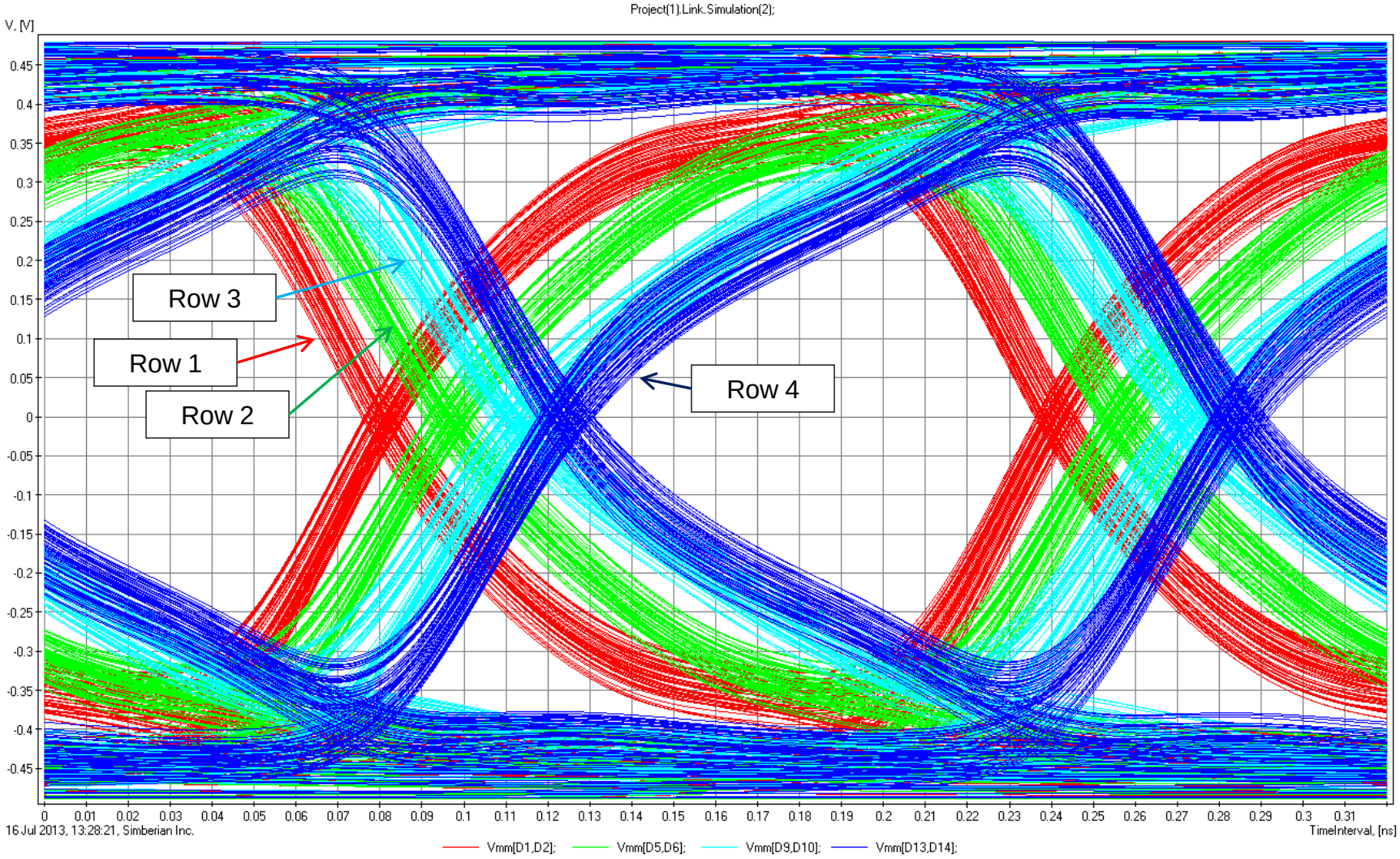
Connector TDR Profile – Row 3



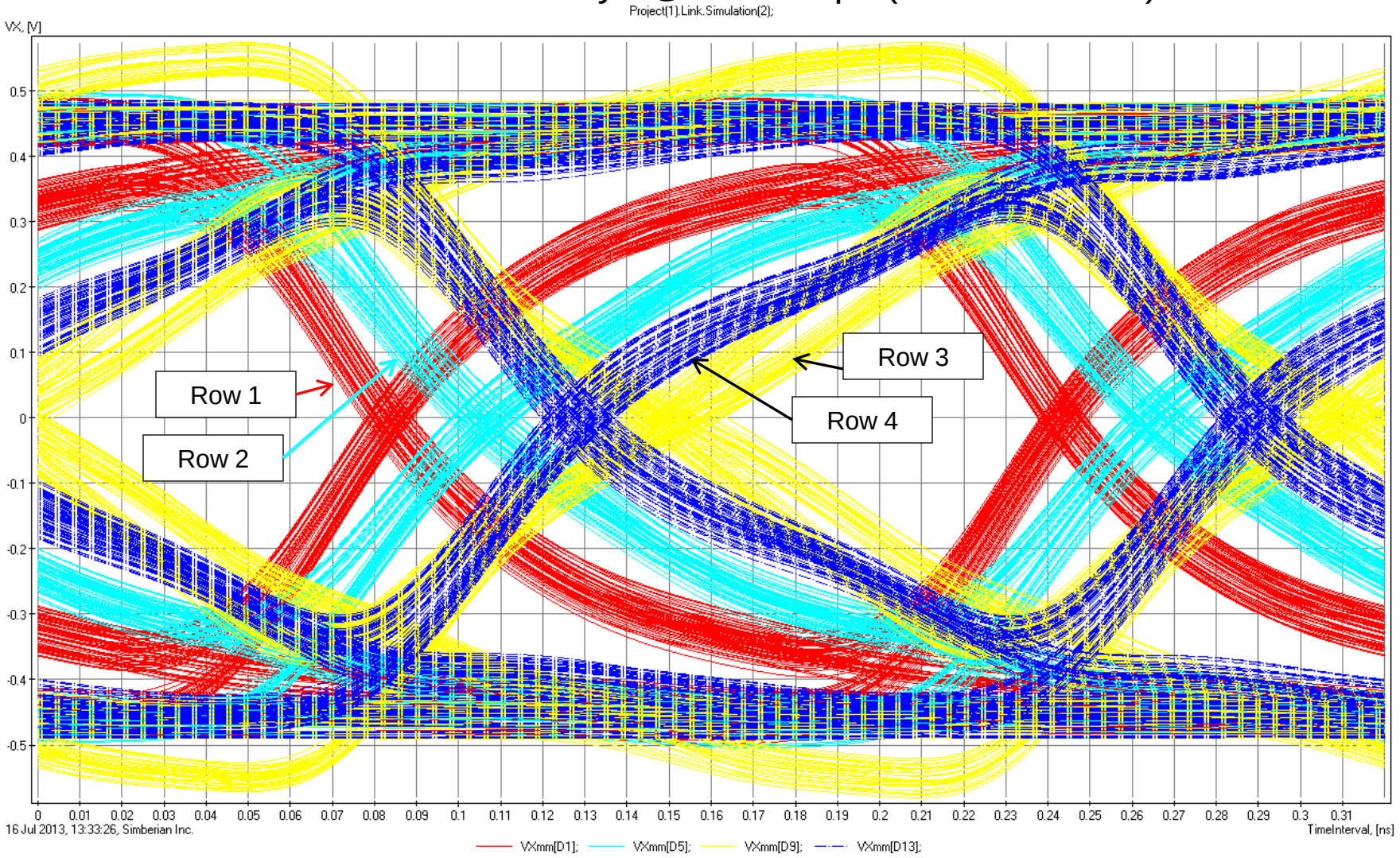
Connector TDR Profile – Row 4



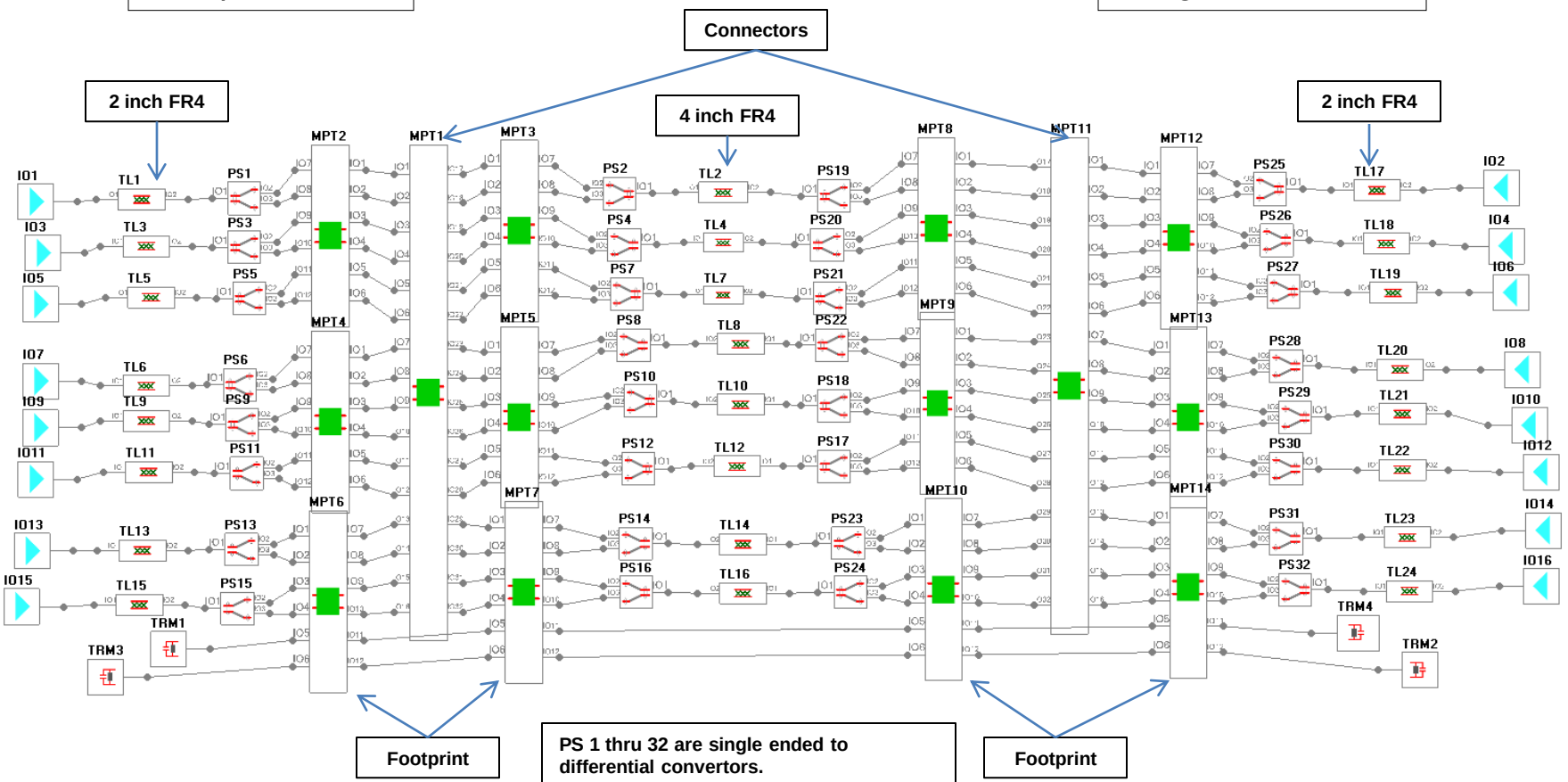
Test Bed Thru Eye @ 6.25 Gbps (No Crosstalk)



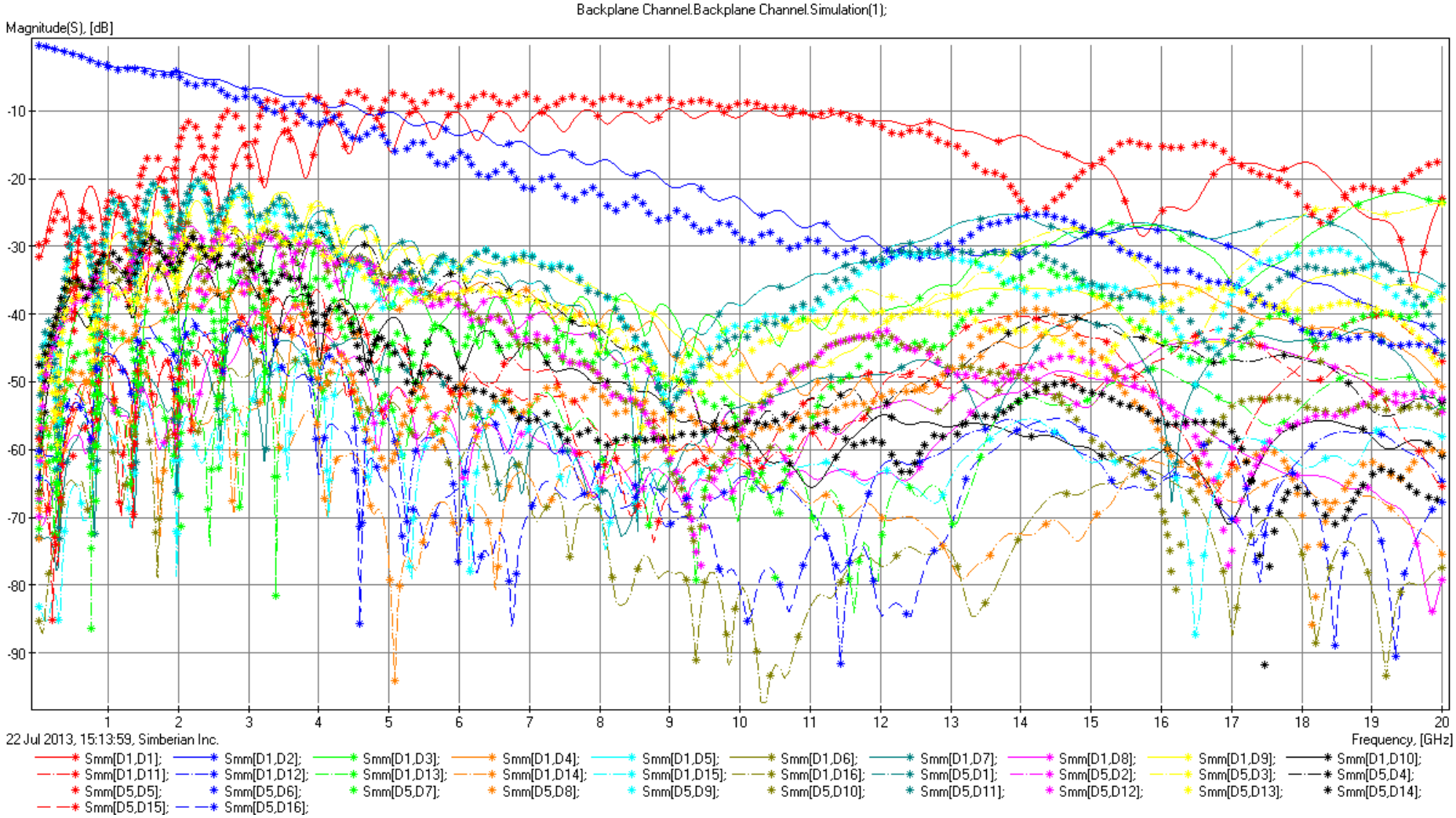
Test Bed Thru Eye @ 6.25 Gbps (With Crosstalk)



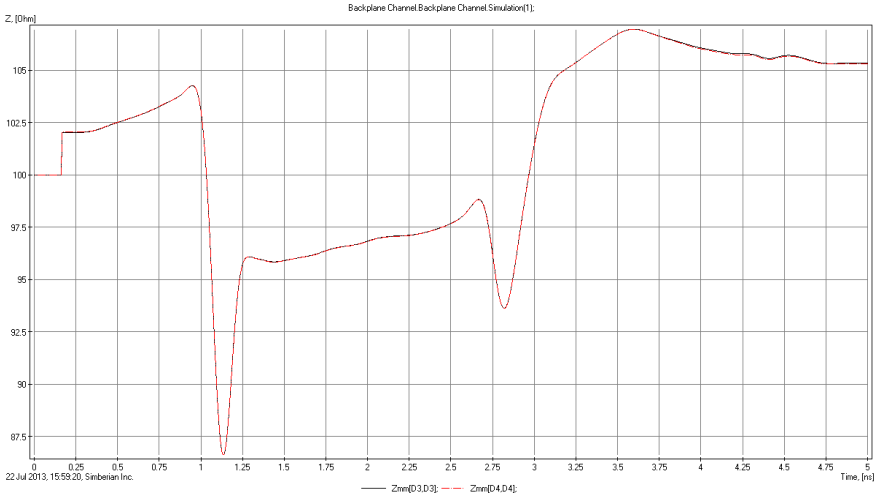
Channel Simulation Schematic



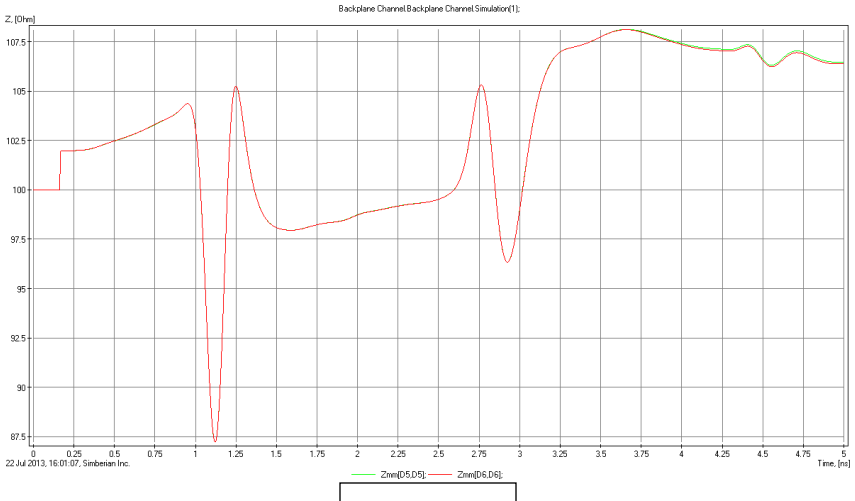
Channel S Parameters



Channel TDR



Row 1



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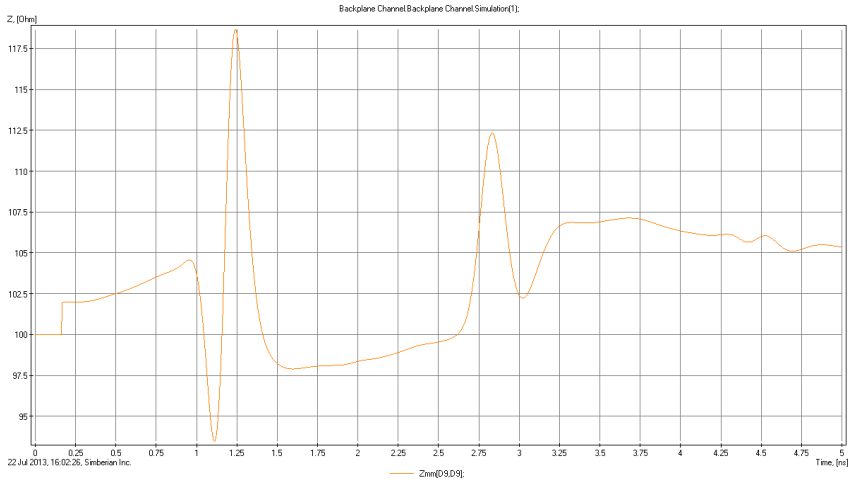

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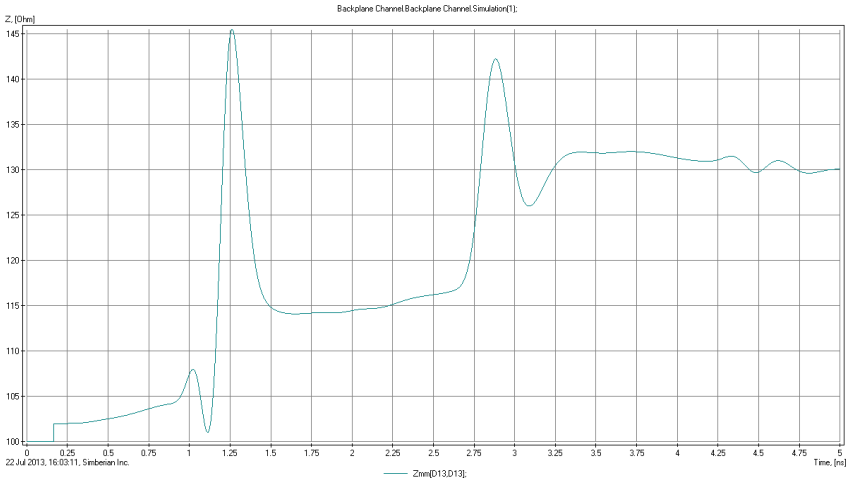
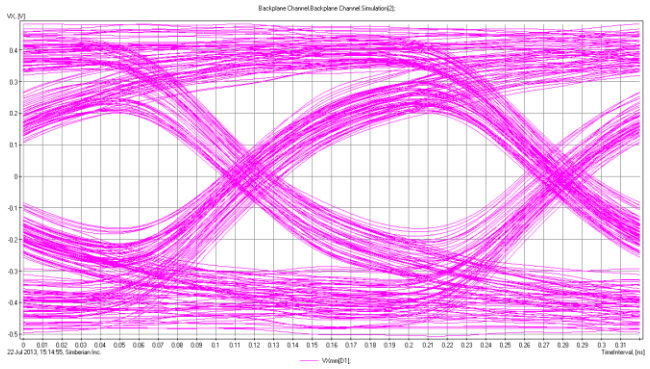
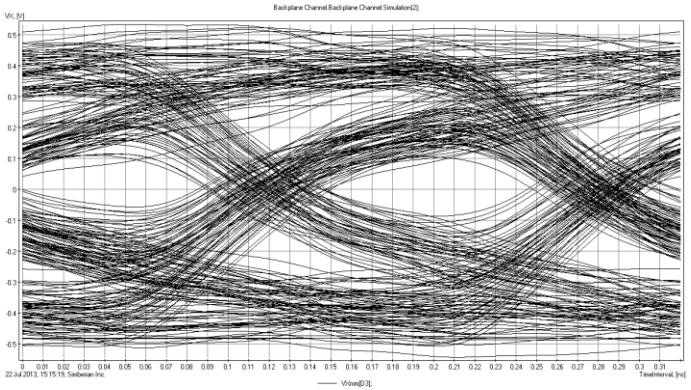


Row 4

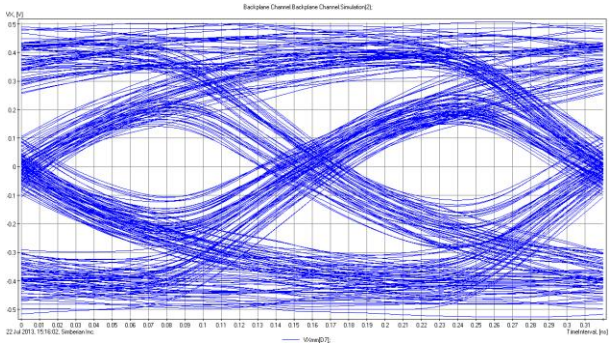
Channel 6.25 Gbps Eye



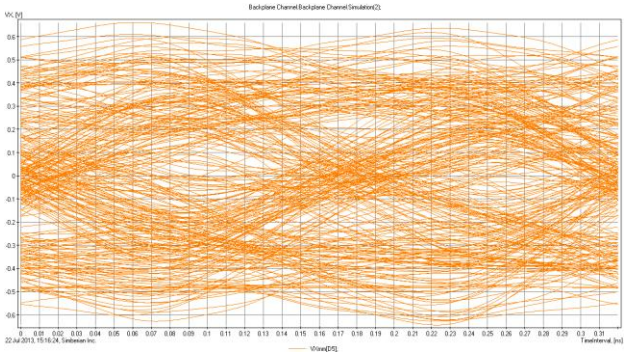
Row 1 – 1 Aggressor



Row 1 – 2 Aggressors

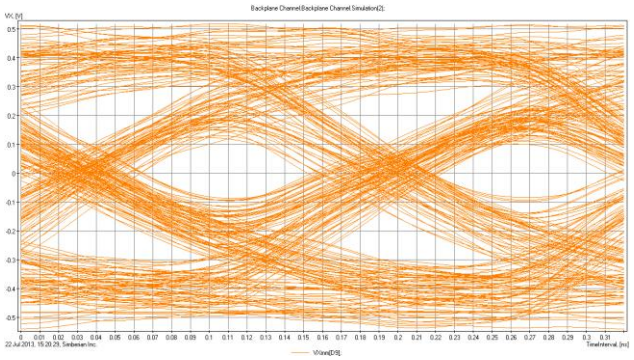


Row 2 – 2 Aggressors

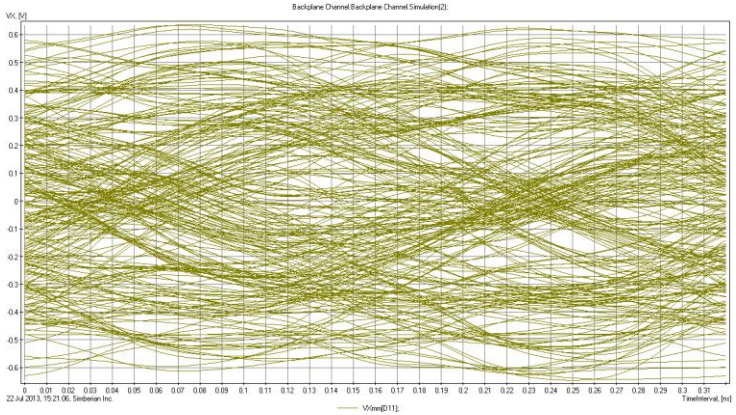


Row 2 – 4 Aggressors

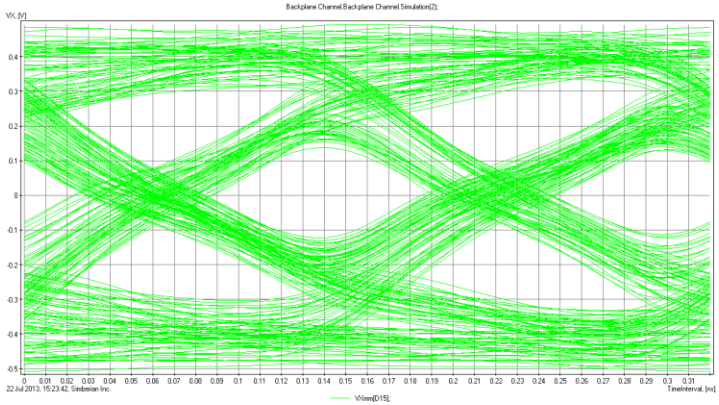
Channel 6.25 Gbps Eye



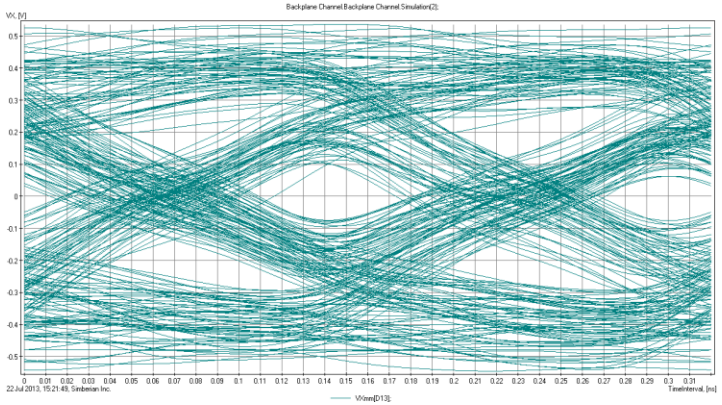
Row 3 – 2 Aggressors



Row 3 – 4 Aggressors



Row 4 – 1 Aggressor



Row 4 – 2 Aggressors